Electronic Version
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[FLASH MEMORY CELL AND MANUFACTURING METHOD THEREOF]

Abstract

A flash memory cell including a p-type substrate, an n-type deep well, a stacked gate structure, a source region, a drain region, a p-type pocket doped region, spacers, a p-type doped region and a contact plug is provided. The n-type deep well is set up within the p-type substrate and the stacked gate structure is set up over the p-type substrate. The stacked gate structure further includes a tunneling oxide layer, a floating gate, an inter-gate dielectric layer, a control gate and a cap layer sequentially formed over the p-type substrate. The source region and the drain region are set up in the p-type substrate on each side of the stacked gate structure. The p-type pocket doped region is set up within the n-type deep well region and extends from the drain region to an area underneath the stacked gate structure adjacent to the source region. The spacers are attached to the sidewalls of the stacked gate structure. The p-type doped region is set up within the drain region. The p-type doped region passes through the junction between the drain region and the p-type pocket doped region but is

separated from the spacer by a distance. The contact plug is set up over the drain region and is electrically connected to the p-type doped region.